Serial to Ethernet Controller with A/D

Features

- Embeds a 8051CPU
- Includes 32KB SSRAM and 64KB OTP ROM
- Includes a 10/100 Ethernet MAC, Ethernet PHY
- Includes 2 channel DMA
- Includes a 7-bit 2 channel ADC(0V~2.5V)
- Provides I2C for EEPROM access
- Includes 3 timers
  - two 8-bit hardware auto load timers
  - one 16-bit hardware auto load timer
- Provides a high speed (up to 921 Kbps) UART(with MODEM control) and 1 simplified UART(Tx, Rx only)
- Supports fiber cable connection
- 0.25um CMOS technology
- 2.5V core and 3.3V (2.5V) IO power
- 48-pin QFN package

General Description

The IP210T is a cost effective and highly integrated Serial-to-Ethernet SoC. Embedding a 8051 CPU, 64KB OTP ROM, 32K bytes SRAM, 2 channel 7-bit ADC, 10/100Mbps Ethernet and UART. The IP210T is targeted for network sensor, Serial-to-Ethernet server and security system.

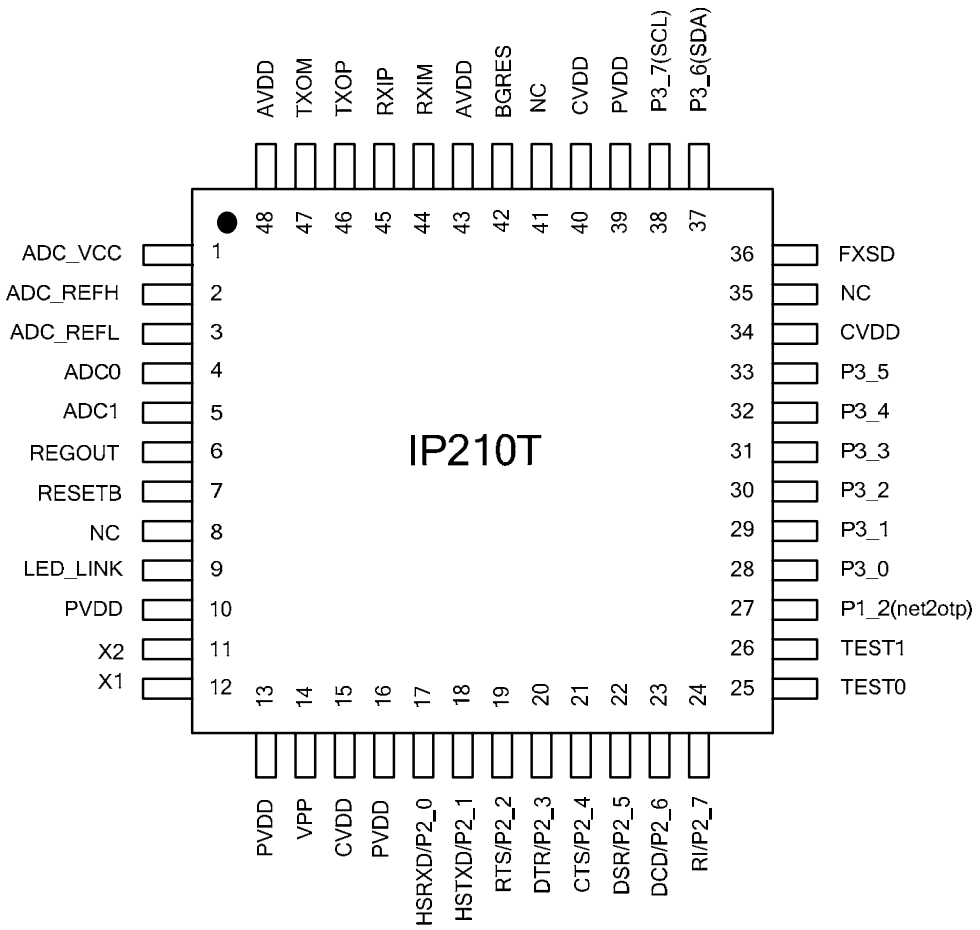
Since all device drivers and protocol stack are embedded inside the SoC, this design provides a neat and cost-effective solution. The 48 pin package allows the designer to build a compact size Serial-to-Ethernet device. 7-bit A/D converter and GPIO pins meet most of design requirements of industrial equipment control. In addition to TP cable connection, the IP210T also provides the fiber cable connection to meet the requirement of long distance communication.

Table of Contents

Revision History

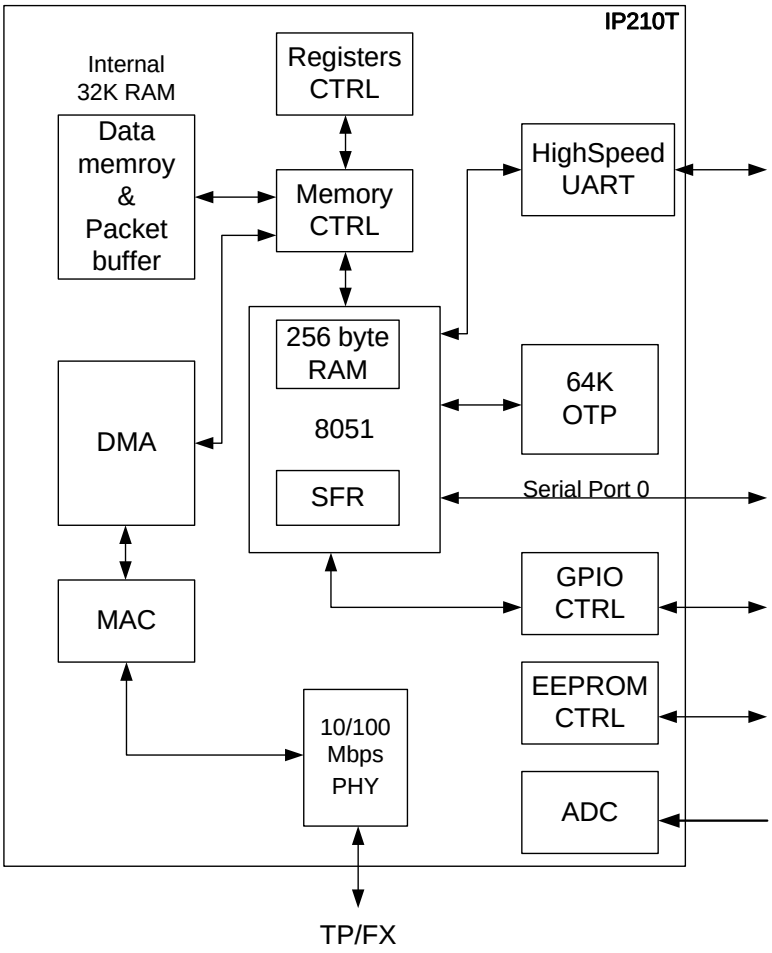
Revision #	Change Description
IP210T-DS-R01	Initial release.

1 Pin Diagram



2 Block Diagram

IP210T block diagram



3 Pin Description

Type	Description
I	Input pin
O	Output pin
IPL	Input pin with internal pull low
IPH	Input pin with internal pull high
P	Power supply

Pin No.	Label	Type	Description
PHY transceiver			
45 44	RXIP RXIM	I/O	**Receive Input Pair** Differential pair shared by 100Base-TX, and 10Base-T modes.
46 47	TXOP TXOM	I/O	**Transmit Output Pair** Differential pair shared by 100Base-TX, and 10Base-T modes. When configured as 100Base-TX, output is an MLT-3 encoded waveform. When configured as 10Base-TX, the output is the Manchester code.
36	FXSD	I	**Fiber signal.** This pin is used to control the operating mode regarding fiber cable. <0.7V: Enable TP cable function. 0.8V ~ 1.6V: Enable fiber cable function. >1.8V: Fiber cable signal detected.

Pin No.	Label	Type	Description
Analog digital converter			
04	ADC0	I	ADC channel 0 analog input
05	ADC1	I	ADC channel 1 analog input
02	ADC_REFH	I	The upper reference voltage. The maximum input voltage range is determined by the voltage applied to ADC_REFH and the voltage applied to ADC_REFL
03	ADC_REFL	I	The lower reference voltage

Pin No.	Label	Type	Description
GPIO 1			
27	P1_2 (net2otp)	IPH/O	P1_2 GPIO 1-2

Pin No.	Label	Type	Description
GPIO 2 & High Speed UART			
17 18 19 20 21 22 23 24	P2_0/HSRXD P2_1/HSTXD P2_2/RTS P2_3/DTR P2_4/CTS P2_5/DSR P2_6/DCD P2_7/RI	IPH/O	This port is either set to MODEM control pin or GPIO pin. All 8 pins should be set to either GPIO mode or MODEM control mode.

Pin No.	Label	Type	Description
GPIO 3			
28 29 30 31 32 33 37 38	P3_0/SRXD0 P3_1/STXD0 P3_2 P3_3/INT1B P3_4/T0(HA[17]) P3_5/T1(HA[16]) P3_6/SDA P3_7/SCL	IPH/O	Port3 is an 8-bit bidirectional I/O port. Port3 also provides various special features listed below: GPIO P3_0 or SRXD0, serial input port 0 GPIO P3_1 or STXD0, serial output port 0 GPIO P3_2 GPIO P3_3 or INT1, External interrupt 1 GPIO P3_4 or T0, Timer 0 external input GPIO P3_5 or T1, Timer 1 external input GPIO P3_6 or SDA, data pin of EEPROM (when (0x8001[4] = 1'b1) GPIO P3_7 or SCL, Clock pin of EEPROM (when (0x8001[4] = 1'b1)

Pin No.	Label	Type	Description
Miscellaneous			
07	RESETB	I	**Reset,** low active. This pin should be kept at “low” state for at least 10 microseconds. Connect this pin to a 1M ohms pull up resistor. There is an internal capacitor between this pin and GND, so the external capacitor is not necessary for a RC reset circuit.
09	CLK25/LINK_LED	IPH/O	CLK25(O)/ LINK_LED(O)
12	X1	I	**System clock input or crystal input** It is recommended to connect X1 and X2 to a crystal. If the clock source is from another chip, the clock should be active at least for 1ms before RESETB de-asserted
11	X2	O	**Crystal output**
42	BGRES	O	Band gap resister. Connect a 6.19K ohms resistor between this pin and the GND.
14	VPP	I	OTP high voltage power (for OTP write). Normal mode: 2.5V. OTP ROM programming mode: 6.5V
06	REGOUT	O	**Regulator Control.** This pin should be connected to the base of a PNP transistor to generate 2.5V output voltage at the collector.
26, 25	TEST1, TEST0	IPH	**Chip Mode Select** **(**1, 1) : normal mode (0, 0) : OTP write mode (1, 0) : reserved (0, 1) : reserved

Pin No.	Label	Type	Description
POWER&GND			
10 13 16 39	PVDD	P	3.3V (2.5V) PAD Power
01	ADC_VCC	P	2.5V Analog Digital Converter Power ADC_VCC should be connected to AVDD (2.5v) even if ADC function is not used
15 34 40	CVDD	P	2.5V Core Power
43 48	AVDD	P	2.5V Analog Power
Exposed-PAD	VSS	P	GND Pad (E-PAD) of IP210T.

4 Function Description

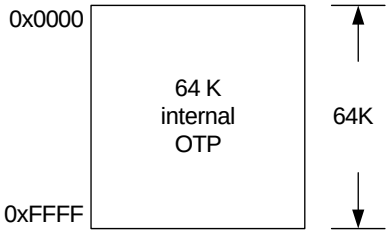
4.1 CPU

4.1.1 Memory organization

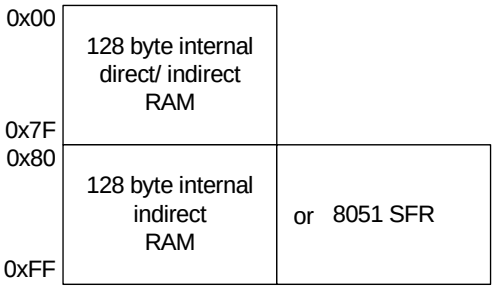
IP210T manipulates operands in three memory spaces: 64KB program memory for internal OTP, 256 bytes 8051 built-in data RAM, and 32KB data memory.

The 256 bytes data RAM space is divided into 256-byte RAM and 128-byte 8051 Special Function Registers (SFR). The lower 128-byte of RAM can be accessed by direct or indirect addressing, the SFR can be access by direct addressing, and the upper 128-byte of RAM can be accessed by indirect addressing only. The 32K data RAM is accessed with instructions different from that for 256-byte RAM.

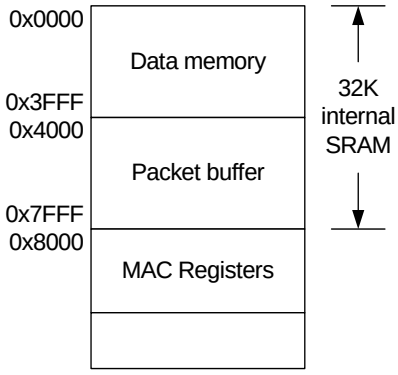
Program memory address map



8051 built-in memory address map



Data memory address map



4.1.2 SFR MAP and Default Value

Address	0 / 8	1 / 9	2 / A	3 / B	4 / C	5 / D	6 / E	7 / F
0xF8								
0xF0	B Register (00000000)							
0xE8	P4 (11111111)							WDTWCYC (00000000)
0xE0	ACC (00000000)	PDCON (XXXXXX01)						
0xD8	WDTCON (01000000)							
0xD0	PSW (00000000)							
0xC8	T2CON (00000000)	T2MOD (00000000)	RCAP2L (00000000)	RCAP2H (00000000)	TL2 (00000000)	TH2 (00000000)		
0xB8	IP (00000000)							
0xB0	P3 (11111111)							
0xA8	IE (00000000)							
0xA0	P2 (11111111)							
0x98	SCON (00000000)	SBUF						
0x90	P1 (11111111)							
0x88	TCON (00000000)	TMOD (00000000)	TL0 (00000000)	TL1 (00000000)	TH0 (00000000)	TH1 (00000000)	**CKCON** (00000000)	
0x80	P0 (11111111)	SP (00000111)	DPL (00000000)	DPH (00000000)	DPL1 (00000000)	DPH1 (00000000)	DPS (XXXXXXX0)	PCON (0XXXXX00)

X bit is reserved bit.

4.1.3 Bit Addressable Registers' Bit definition

Reg Address	Reg Name	Bit Address							
		0	1	2	3	4	5	6	7
0xD8	**WDTCON**	WDTRST	WDTEN	HWWDT_CLR	HWWDT_DIS	Flash_Access_En			
0xD0	**PSW**	PARITY	F1	OV	RS0	RS1	F0	AC	CY
0xC8	**T2CON**	CP/RL2	C/T2	TR2	EXEN2	TCLK	RCLK	EXF2	TF2
0xB8	**IP**	PX0	PT0	PX1	PT1	PS	PT2	PS1	
0xB0	**P3**	RXD	TXD	INT0	INT1	T0 (Bank A17)	T1 (Bank A18)		
0xA8	**IE**	EX0	ET0	EX1	ET1	ES	ET2	ES1	EA
0x98	**SCON**	RI	TI	RB8	TB8	REN	SM2	SM1	SM0
0x90	**P1**			RXD1	TXD1				
0x88	**TCON**	IT0	IE0	IT1	IE1	TR0	TF0	TR1	TF1

4.1.4 Non Bit Addressable Registers' Bit definition

Reg Address	Reg Name	Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7
0xC9	**T2MOD**	DCEN	T2OE						
0x89	**TMOD**	M0	M1	C/T	GATE	M0	M1	C/T	GATE
0x87	**PCON**	IDL	PD						SMOD
0xE1	**PDCON**	PDC	JWP						
0x8E	**CKCON**	MD0	MD1	MD2	T0M	T1M	T2M	WDT0	WDT1

4.1.5 Register Description (Non 8051 standard registers)

<table>
<tr><th>Address</th><th>Register Name</th><th>Access</th><th>Description</th></tr>
<tr><td>0x8E</td><td>CKCON</td><td>RW</td><td>Power-down Control register
Bit0-2: Insert wait state for MOVX
<table>
<tr><td>MD2</td><td>MD1</td><td>MD0</td><td>Wait state</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>8</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>12</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>16</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>20</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>24</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>28</td></tr>
</table>
Bit3: Timer0 clock = system clock /4 or /12 (1/0)
Bit4: Timer1 clock = system clock /4 or /12 (1/0)
Bit5: Timer2 clock = system clock /4 or /12 (1/0)
Bit6-7: WDT time-out counter select
<table>
<tr><td>WDT1</td><td>WDT0</td><td>Counter width</td></tr>
<tr><td>0</td><td>0</td><td>17</td></tr>
<tr><td>0</td><td>1</td><td>20</td></tr>
<tr><td>1</td><td>0</td><td>23</td></tr>
<tr><td>1</td><td>1</td><td>26</td></tr>
</table></td></tr>
<tr><td>0xE1</td><td>PDCON</td><td>RW</td><td>Power-down Control register
Bit 0: PDC (Power Down Control)
0 – pull high of P1/P2/P3 when entering power-down mode
1 – pull low of P1/P2/P3 when entering power-down mode
Bit 1: JWP (Just Wake Up, it works not only in PowerDown mode, but also in Idle mode)
0 – issue interrupt after WakeUp
1 – don't issue interrupt after WakeUp
Bit2-7: reserved</td></tr>
<tr><td>0xD8</td><td>WDTCON</td><td>RW</td><td>Watch-dog control register
Bit0: (WDTRST): Watch-dog reset
Bit1: (WDTEN): Watch-dog enable
Bit2: (HWWDT_CLR): Hardware Watch-dog clear
Bit3: (HWWDT_DIS): Hardware Watch-dog disable
Bit4: Flash_Access_En</td></tr>
</table>

			0- default 1- redirect XDATA Bus to Flash's Address & DATA Bus Bit5-6: reserved Bit7: SMOD_1 – Serial modification. Double baud rate of serial port 1 if this bit set 1.
0xC8	T2CON	RW	Control register of Timer 2
0xC9	T2MOD	RW	Mode register of Timer 2 Bit0:T2OE(Timer2 Output Enable) Switching Timer 2 clock-out mode, which connects the programmable clock output to external pin T2. Bit1:DCEN(Down Count Enable) 1: Timer 2 as Down counter. 0: Timer 2 as Up counter.(default)
0xCA	RCAP2L	RW	Low byte of Timer 2 re-load register
0xCB	RCAP2H	RW	High byte of Timer 2 re-load register
0xCC	TL2	RW	Low byte of Timer 2 register
0xCD	TH2	RW	High byte of Timer 2 register
0xE8	P4	RW	General Purpose IO
0xEF	WDTWCYC	RW	For every (WDTWCYC+1) system clocks, CPU advances WDT by 1. Used with Watch Dog Timer for easier Time Control.

4.1.6 Register description (8051 standard registers)

Address	Register Name	Access	Description
0x87	PCON	RW	Power Control register: Bit 7- SMOD: this bit is used to double the baud rate when TIMER 1 is used to generate baud rate and Serial port is set in mode 1/2/3
0x98	SCON	RW	Serial Port Control Register: Bit [7:6] : Serial Port mode 00-Shift Register Baud Rate=Fosc/12 01-8 bit Baud Rate=variable 10-9 bit Baud Rate=Fosc/64 or Fosc/32 11-9 bit Baud Rate=variable Bit5: Enable Multi-processor communication Bit4: Rx_Enable Bit3: the 9th bit TX value when bit[7:6]=10/11 Bit2: the 9th bit RX value when bit[7:6]=10/11 Bit1(TI) : TX Interrupt Status H/W set TI=1 when H/W has sent out data in SBUF. Bit0(RI) : RX Interrupt Status H/W set RI=1 when H/W has received data in SBUF.
0x99	SBUF	RW	Serial Port Buffer: store the data to be transmitted out or received in.
0xA8	IE	RW	Interrupt Enable: Bit7: 0- disable all interrupts 1- each interrupt source is individually enabled or disabled by setting or clearing its enable bit Bit6: 0 - disable Serial Port 1 interrupt(RI_1/TI_1) 1 - enable Serial Port 1 interrupt

			Bit5: 0 - disable Timer 2 interrupt 1 - enable Timer 2 interrupt Bit4: 0 - disable Serial Port interrupt(RI/TI) 1 - enable Serial Port interrupt Bit3: 0 - disable Timer 1 interrupt 1 - enable Timer 1 interrupt Bit2: 0 - disable External 1 interrupt 1 - enable External 1 interrupt Bit1: 0 - disable Timer 0 interrupt 1 - enable Timer 0 interrupt Bit0: 0 - disable External 0 interrupt 1 - enable External 0 interrupt
0xB8	IP	RW	Interrupt Priority: For each interrupt, 1 is high priority and 0 is low priority.
0x88	TCON	RW	Timer Control Register.
0x89	TMOD	RW	Timer Mode Control Register.
0x8A	TL0	RW	Timer0 LSB.
0x8B	TL1	RW	Timer1 LSB.
0x8C	TH0	RW	Timer0 MSB.
0x8D	TH1	RW	Timer1 MSB.
0x83	DPH	RW	DPTR MSB.
0x82	DPL	RW	DPTR LSB.
0x81	SP	RW	Stack Pointer.
0x80	P0	RW	General Purpose IO
0x90	P1	RW	General Purpose IO
0xA0	P2	RW	General Purpose IO
0xB0	P3	RW	General Purpose IO

4.1.7 CPU Interrupt

IP210T supports both hardware interrupt and software interrupt. The following table shows the interrupt types which are implemented in IP210T.

The only one difference between IP210T and standard 8051 about the interrupt is that INT0 pin for external interrupt0 trigger is no longer exist, the interrupt0 is designed to be the interrupt sourcing from Network TX/RX, DMA, Timer/Counter overflow, High Speed UART, ADC and PHY status. Besides IE0, to enable each interrupt the individual enable bit of Interrupt Enable Register (0x8004) should be set, and the Status Register (0x8003) would show the status for each interrupt. When an interrupt is generated, the Interrupt Service Routine (ISR) will check the interrupt source by checking Status Register to know what interrupt is occurring.

Since the interrupt function of External request 0 is designed to respond only to the joint events of Interrupt Enable Register & Interrupt Status Register, pin P3.2 on IP210T is no longer used as the INT0 pin for External Request 0.

Interrupt Source	Vector Address	Request Flag	Enable Flag
External Request0 (High Speed UART, Ethernet TX/RX, DMA, ADC, Timer/Counter Overflow and PHY)	0003h	Status Register (0x8003)	Interrupt Enable Register (0x8004) and EX0
Timer0	000Bh	TF0/TCON.5	ET0/IE.1
External Request1	0013h	IE1/TCON.3	EX1/IE.2
Timer1	001Bh	TF1/TCON.7	ET1/IE.3
Serial Port0	0023h	T:TI/SCON.1, R:RI/SCON.0	ES/IE.4
Timer2	002Bh	TF2/T2CON.7	ET2/IE.5

4.1.8 CPU Timers/Counters

Like a standard 8052, there are three timers/counters inside IP210T. SFR TMOD & TCON are used to configure the operation modes of Timer0 and Timer1. SFR T2MOD & T2CON are used to configure Timer2's operation modes.

4.1.8.1 Timer0

Timer0 is a 16-bit timer/counter and functions just like one of a standard 8051.

TMOD.bit1	TMOD.bit0	MODE	Description
0	0	0	8-bit timer/counter(TH0) with 5-bit prescalar(TL0).
0	1	1	16-bit timer/counter.
1	0	2	8-bit auto-reload timer/counter(TL0), reload from TH0 at overflow.
1	1	3	TL0 is an 8-bit timer/counter. TH0 is an 8-bit timer using timer1's TR1 and TF1 bits.

Note: Only one difference of Timer0 to the timer0 of standard 8051 is the INT0 pin no longer exist. Therefore, Gate bit(TMOD.bit3) for timer0 can't be used to control the operation of timer0 as TR0 is turned on.(Please refer to CPU Interrupt section)

4.1.8.2 Timer1

Timer1 is a 16-bit timer/counter and functions just like one of a standard 8051

TMOD.bit5	TMOD.bit4	MODE	Description
0	0	0	8-bit timer/counter(TH1) with 5-bit prescalar(TL1).
0	1	1	16-bit timer/counter.
1	0	2	8-bit auto-reload timer/counter(TL1), reload from TH1 at overflow.
1	1	3	Timer1 halted,

4.1.8.3 Timer2

It's a 16-bit Timer and SFR T2MOD & T2CON are used to control its operations. It can count up & count down depending on TMOD.bit0 (DCEN). T2 pin is multiplexed through P1.5 and T2EX is multiplexed through P1.6. The operation modes of Timer2 are shown as follows.

SFR 0xc8	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
T2CON	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/~T2	CP/~RL2

When C/~T2 bit (T2CON.bit1) is set to 1, it operates as a counter and is triggered by T2 pin.
When EXEN2 bit (T2CON.bit3) is set to 1, a negative edge of T2EX will set EXF2 (T2CON.bit6) to 1 and cause a capture or a reload on Timer2.

SFR 0xc9	**bit 7**	**bit 6**	**bit 5**	**bit 4**	**bit 3**	**bit 2**	**bit 1**	**bit 0**
T2MOD							T2OE	DCEN

Mode		**Description**
Auto-Reload	T2MOD.bit0(CP/~RL2=0)	16-bit timer. TL2&TH2 are reloaded from RCAP2L&RCAP2H when overflow.
Capture	T2MOD.bit0(CP/~RL2=1)	16-bit timer. TL2&TH2 are captured to RCAP2L&RCAP2H when overflow. T2EX (P1.6) triggers the capture operation.

<table>
<tr><td>Baud rate Generator</td><td>T2CON.RCLK
T2CON.TCLK</td><td>As the Baud rate Generator for Serial Ports by setting RCLK&TCLK bits of SFR T2CON.
<table>
<tr><th>RCLK</th><th>TCLK</th><th>Receiver Baud rate Generator</th><th>Transmitter Baud rate Generator</th></tr>
<tr><td>0</td><td>0</td><td>Timer1</td><td>Timer1</td></tr>
<tr><td>0</td><td>1</td><td>Timer1</td><td>Timer2</td></tr>
<tr><td>1</td><td>0</td><td>Timer2</td><td>Timer1</td></tr>
<tr><td>1</td><td>1</td><td>Timer2</td><td>Timer2</td></tr>
</table></td></tr>
<tr><td>ClockOut</td><td>T2OE=1</td><td>T2 (P1.5) outputs 50/50 duty-cycle clock. Its frequency is determined by the overflow rate of Timer2.</td></tr>
<tr><td>DownCount</td><td>DCEN=1</td><td>Timer2 counts down.</td></tr>
</table>

ClockOut Frequency = 58.9 MHz/ (4*(65536-16bit_timer_value))

4.1.9 CPU Mirror Mode

4.1.9.1 Purpose

It's used to redirect CPU's Code Space into XDATA Space (Internal Memory), so that CPU fetches the instructions from internal Memory instead of the external Flash Memory.

4.1.9.2 Action

When ChipConfigure Register_0.bit5 (Mirror_En) is set to 1, CPU runs in Mirror Mode. Before CPU enters Mirror Mode, the code data to be run should be moved to the internal Memory. In Mirror Mode, if the content of Mirror_Address_Register (0x8006) is 0xE0, CPU sees the Internal Memory address 0x0000 as 0xE000 of its Code Space. For example, if CPU fetches an instruction at address 0xE005 of Code Space, it returns the content of address 0x0005 of Internal Memory.

4.1.10 Power Management

4.1.10.1 Idle Mode

When PCON.IDL=1, IP210T enters Idle mode. In idle mode, IP210T's CPU is idle but all the peripherals remain active. The internal RAM and SFR registers remain unchanged too. The idle mode can be terminated by any enabled interrupt.

4.1.10.2 Power Down Mode

When PCON.PD=1, IP210T will enter power-down mode. The system clock is stopped in this mode. This mode can be wakened up by external enabled interrupt (EX1) with level trigger configuration (TCON.IT0=0 or TCON.IT1=0). The Program Counter, internal RAM and SFR registers retain their values no changed after resume from Power Down mode.

The GPIO1 ~ GPIO3 will be pulled high or low that depends on the setting of PDCON.PDC after entering Power Down mode.
For example, when PDCON.PDC=0, GPIO0 ~ GPIO3 will be 0xFF.

4.1.11 Watch Dog Timers

There are two Watch Dog Timers employed to protect user programs from unexpectedly shutting down while IP210T has been through severe environmental problems. When user program somehow shuts down or works in a unexpected manner, the overflow of WDTs can reset the system and restart user program.

0xD8	WDTCON	WDTRST	WDTEN	HWWDT_CLR	HWWDT_DIS				

4.1.11.1 Watch Dog Timer 1, WDT

0x8E	CKCON							WDT0	WDT1

WDT0(CKCON.bit6) & WDT1(CKCON.bit7):Used to select the counter widths of WDT as shown in CKCON definition.
WDTRST(WDTCON.bit0): Write 1 to this bit clears WDT to zero, preventing from WDT overflow.
WDTEN(WDTCON.bit1): Set this bit to 1 makes WDT counter increase following system clock.
WDTWCYC: Set value ranging from 1 to 255 inserts the value of wait cycle when counting WDT. For example, if this value is 0, WDT counts up for every system clock. If the value is 1, WDT counts up for every 2 system clock. If the value is 7, WDT counts up for every 8 system clock. And so forth.

4.1.11.2 Watch Dog Timer 2, HWWDT

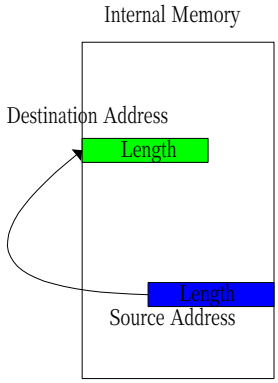
This WDT is enabled by default when IP210T's powered on.
HWWDT_CLR: Write 1 to this bit and then write 0 to this bit clears HWWDT, preventing from HWWDT overflow. Program should write this bit twice(write 0 and write 1) in a very short time.
HWWDT_DIS: Set this bit to 1 stops HWWDT from counting.

4.2 DMA

4.2.1 Internal memory to internal memory

4.2.1.1 Purpose

This function is used to move an amount of data from one internal Memory location to another.



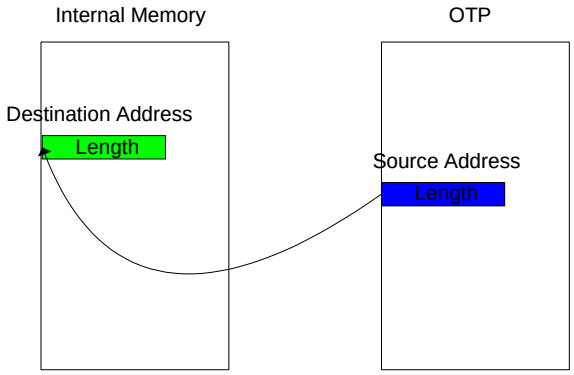
4.2.1.2 Action

a. Initialize DMA_Source_Address, DMA_Destination_Address and DMA_Length registers.
b. Write 0x1 to DMA_COMMAND register to invoke Internal Memory to Internal Memory DMA operation.
c. IP210T starts this operation. When it's done, IP210T sets DMA_COMMAND=0 and StatusRegister.bit2=1.
d. Firmware keeps on polling the content of DMA_COMMAND register. When it becomes 0x0, this DMA operation is finished.

4.2.2 OTP to internal memory

4.2.2.1 Purpose

This function is used to move an amount of data from OTP into internal Memory.



4.2.2.2 Action

a. Initialize DMA_Source_Address, DMA_Destination_Address and DMA_Length registers.
b. Set CPU SFR EA=1 and Ex0=1 to enable external request interrupt so that an interrupt will occur to bring CPU out of IDLE mode when DMA operation's done.
c. Set Interrupt_EnableRegister.bit2=1 to allow an interrupt caused by DMA operation.
d. Write 0x4 to DMA_COMMAND register to tell IP210T an OTP to internal Memory DMA operation will be started.
e. Set PDCON.bit1 (JWP) =1 to not execute Interrupt Vector after
f. Set SFR PCON.bit0 (IDL) to 1 to switch CPU to IDLE mode.
g. After switching to IDLE mode, IP210T starts this operation.

h. When this operation is done, IP210T sets StatusRegister.bit2=1 to generate an external request interrupt to bring CPU back from IDLE mode. IP210T sets DMA_COMMAND to 0x0.

4.3 Timer/Counter

4.3.1 Purpose

To maintain a real-time counter on IP210T.

Related Registers
Timer Counter Register latch enable
Timer Counter Register_0 (LSB)
Timer Counter Register_1
Timer Counter Register_2
Timer Counter Register_3 (MSB)

4.3.2 Initialize real-time counter

a. Set CPU's Timer/Counter2 to 16bit auto-reload mode. Then make Timer/Counter2 run to generate overflows with fixed time interval.
b. Write an initial value to Timer Counter Register, such as 0x0000.
c. Timer Counter Register increments every time Timer/Counter2 wraps around from 0xFFFF to 0x0000.

4.3.3 Read real-time counter

a. Write 0x1 to **Timer Counter latch enable** register to latch real-time counter to Timer Counter Register.
b. Read Timer Counter Registers.

4.3.4 Timer/Counter overflow

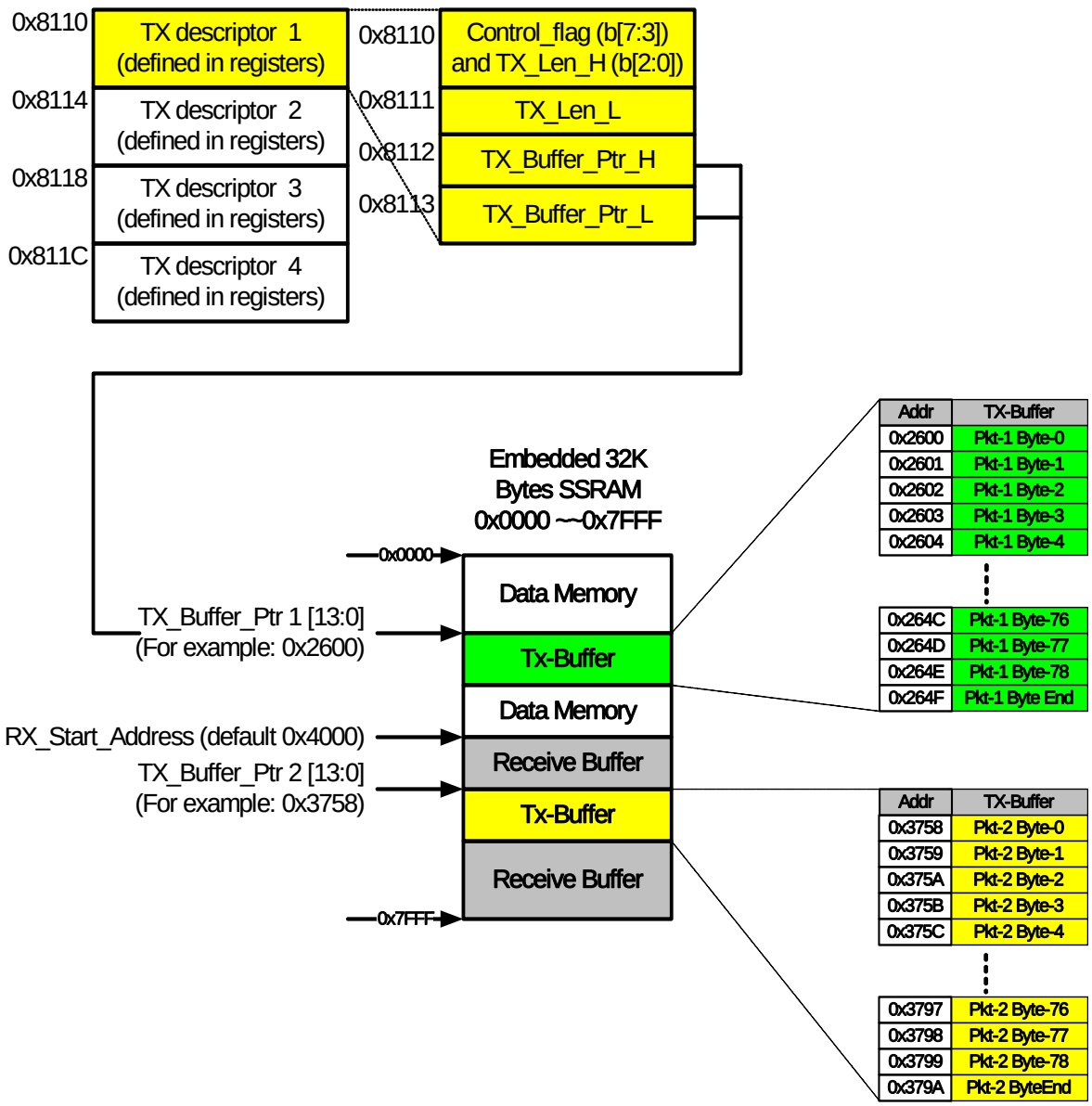
When the real-time Timer/Counter wraps around from 0xffffffff to 0x00000000, IP210T sets StatusRegister.bit3=1 to notify Firmware (by Polling to StatusRegister or EX0 Interrupt).

4.4 MAC

4.4.1 TX MAC

4.4.1.1 TX descriptor registers

IP210T provides 4 TX descriptors as follows.



4.4.1.2 IP Checksum and CRC32 calculation for a proprietary packet

In some applications, the proprietary packet with special tag may be necessary. Because of the variable length of the tag field, IP210T can't calculate the IP checksum or CRC excluding the tag field automatically. To solve this problem, IP210T supports a DMA function to calculate IP Checksum and CRC32

4.4.2 RX buffer

RX Buffer is a block of internal 32K SSRAM for MAC to store the received frames. Its area is from the value of RX buffer start address to the end address of internal RAM (16Kbytes). It is a ring buffer. When the frame crosses the boundary of internal RAM, the MAC will automatically wrap around to the start address of RX Buffer.

4.4.2.1 RX Filter

IP210T supports two RX filter registers, RX_Filter_Registers_0 and RX_Filter_Registers_1. IP210T receives a packet if it meets any one of the conditions turned on in RX_Filter_Registers_0. IP210T receives a packet if it meets all of the conditions turned on in RX_Filter_Registers_1.

4.5 EEPROM I/F

4.5.1 Configuration

4.5.1.1 Access through P3[7:6]

IP210T supports access to EEPROM through SCL and SDA pins. If Chip Configure Register_1[4:3] =2'b10(P3_I2C_En=1, P4_I2C_En=0), EEPROM function is enabled and P3.7=SCL & P3.6=SDA.

4.5.1.2 Supported EEPROM types

EEPROM types	24C01	24C02	24C04	24C08	24C16
Read Page Max Byte Count	32	32	32	32	32
Write Page Max Byte Count	8	8	16	16	16

4.5.2 Related Registers

EEPROM_Data_Register
EEPROM_Addresss_Register
EEPROM_ID_Register
EEPROM_Command_Register
EEPROM_Control_Register

4.5.3 Address of EEPROM

EEPROM types	24C01	24C02	24C04	24C08	24C16
EEPROM_Addresss_Register	Address[7:0]	Address[7:0]	Address[7:0]	Address[7:0]	Address[7:0]
EEPROM_ID_Register.bit0	0	0	Address[8]	Address[8]	Address[8]
EEPROM_ID_Register.bit1	0	0	0	Address[9]	Address[9]
EEPROM_ID_Register.bit2	0	0	0	0	Address[10]
EEPROM_ID_Register.bit[7:3]	0	0	0	0	0

4.6 UART

There are two kinds of UARTs in IP210T. One is the standard 8051-built-in UART without FIFO (Serial Port0). Its control registers is in SFR. The other one is 16C650 compatible UART designed with FIFO and can support high-speed data transfer up to 921.6kbps (determined by Divisor Register).

4.6.1 The operation of the UART in 8051

4.6.1.1 Serial Port0

P3.0(RXD) and P3.1(TXD) are used to perform data transfer through Serial Port0. SCON(0x98), PCON(0x87).bit7(SMOD) and SBUF(0x99) are SFRs that control its communication operations just like what it's like in a standard 8051. If needed, IE(0xA8).bit4(ES) is used to activate interrupt.

4.6.1.2 Modes

This Baud rate clock source can be from Timer1 or Timer2 of 8051. Like standard 8051, Serial Port0 can support four operation modes as the table shown below. .

SM0	SM1	Mode	Function	Baud rate
0	0	0	Synchronous Mode	Sys_CLK/12
0	1	1	8bit-UART	Variable
1	0	2	9bit-UART	Sys_CLK/64 or Sys_CLK/32
1	1	3	9bit-UART	Variable

4.6.2 The operation of High Speed UART with FIFO

This High Speed UART is compatible with 16C650 UART, which supports full set of MODEM control signals. By setting the Divisor Register, it can support data transfer rate up to 921.6kbps baud rate.

4.6.2.1 Enable High Speed UART

After Chip_Configure_1_Register.bit1(HSP_UART_En) is set to 1, GPIO 2(P2) is switched to act as a high speed UART operations. Its pin mapping is as follows:

P2.0	HSRXD
P2.1	HSTXD
P2.2	RTS
P2.3	DTR
P2.4	CTS
P2.5	DSR
P2.6	DCD
P2.7	RI

4.6.2.2 Related Registers' Briefing

(Detailed definition can be found in IO Register Map)

A. Interrupt Enable Register (IER)

When one of bit0-bit4 of this register is set to 1, any related event will set STATUS.bit4 (HighSpeed_UART_Status_change) to 1, enabling the corresponding interrupt source.

B. Interrupt Identification Register (IIR)

When an UART interrupt is issued, this register should be checked to know which event has occurred.

C. FIFO Control Register (FCR)

Bit0 is used to reset UART Receive module and bit1 is used to reset UART Transmit module. Bits[7:2] is used to determine the threshold number of bytes in FIFO required to enable the Received Data Available interrupt.

D. Line Control Register (LCR)

The line control register allows the specification of the format of the asynchronous data communication used, including the number of bits in a character, stop bit and parity setting. Bit7 is used to control the write action to Divisor register.

E. Modem Control Register (MCR)

The modem control register allows transferring control signals to a modem connected to the UART.

F. Line Status Register (LSR)

This register is used to tell the some status of UART, especially some error or notable events.

G. Modem Status Register (MSR)

The register displays the current state of the modem control lines

H. UART_RX_FIFO_STATUS

Read this register to get the current number of data received in the RX FIFO.

I. UART_TX_FIFO_STATUS

Read this register to get the max number of data that is allowed to push into TX FIFO before it turns full.

J. UART_Receiver Buffer

IP210T owns 256 bytes of UART Receive FIFO buffer. Read UART_Receiver_Buffer Register to get a byte of received data from Receive FIFO. After a read access to this register, the number of data in FIFO is decreased by one.

K. UART_Transmit Buffer

IP210T owns 256 bytes of UART Transmit FIFO buffer. Write UART_Transmit_Buffer Register to put a byte of data to Transmit FIFO. After a write access to this register, the number of data in FIFO is increased by one.

L. Divisor

The value of Divisor allows the selection of UART baudrate. Baudrate=(58.9M)/(16*divisor) bps.

4.7 IP210T OTP ROM

4.7.1 Burning OTP Memory

The following procedures are required to program the OTP memory.

(1) Set Test[1:0] pins to “00”.

(2) Input 6.5V power source to VPP pin.

4.8 PHY Transceiver Interface

4.8.1 Registers definition

Register	Description
0	Control Register
1	Status Register
2	PHY Identifier 1 Register
3	PHY Identifier 2 Register
4	Auto-Negotiation Advertisement Register
5	Auto-Negotiation Link Partner Ability Register
6	Auto-Negotiation Expansion Registers

4.8.2

4.8.3 Register0 : Control Register

Reg.bit	Name	Description	Mode	Default
0.[15]	Reset	1=PHY reset. This bit is self-clearing.	RW/SC	0
0.[14]	Loopback	1=Enable loopback. This will loopback TXD to RXD internally 0=Normal operation.	RW	0
0.[13]	Spd_Sel	1=100Mbps 0=10Mbps When Nway is enabled, this bit reflects the result of auto-negotiation. (Read only) When Nway is disabled, this bit can be set by SMI. (Read/Write)	RW	1
0.[12]	Auto Negotiation Enable	1 = Enable auto-negotiation process. 0 = disable auto-negotiation process. This bit can be set through SMI.	RW	1 or 0 for 100FX
0.[11]	Power Down	1=Power down. All functions will be disabled except SMI . 0=Normal operation.	RW	0
0.[10]	Isolate	1 = Electrically isolate the PHY from RMII/SMII PHY is still able to respond to MDC/MDIO. 0 = Normal operation	RW	0
0.[9]	Restart Auto Negotiation	1=Restart Auto-Negotiation process. 0=Normal operation.	RW/SC	0
0.[8]	Duplex Mode	1=Full duplex operation. 0=Half duplex operation. When Nway is enabled, this bit reflects the result of auto-negotiation. (Read only) When Nway is disabled, this bit can be set through SMI (Read/Write). When 100FX is enabled, this bit can be set through SMI. (Read/Write).	RW	0
0.[7:0]	Reserved			0

4.8.4 Register1 : Status Register

Reg.bit	Name	Description	Mode	Default
1.[15]	100Base_T4	0 = no 100Base-T4 capability.	RO	0
1.[14]	100Base_TX_FD	1=100Base-TX full duplex capable. 0=not 100Base-TX full duplex capable.	RO	1
1.[13]	100Base_TX_HD	1=100Base-TX half duplex capable. 0=not 100Base-TX half duplex capable.	RO	1
1.[12]	10Base_T_FD	1=10Base-TX full duplex capable. 0=not 10Base-TX full duplex capable.	RO	1
1.[11]	10Base_T_HD	1=10Base-TX half duplex capable. 0=not 10Base-TX half duplex capable.	RO	1
1.[10:7]	Reserved		RO	0
1.[6]	MF Preamble Suppression	The PHY will accept management frames with preamble suppressed. PHY accepts management frame without preamble. Minimum of 32 preamble bits are required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions (as defined in IEEE802.3u spec).	RO	1
1.[5]	Auto-negotiate Complete	1=Auto-negotiation process completed. Reg.4,5 are valid if this bit is set. 0=Auto-negotiation process not completed.	RO	0
1.[4]	Remote Fault	1=Remote fault condition detected. 0=No remote fault. In 100FX mode, this bit means the in-band signal Far-End-Fault is detected. Refer to FX MODE section.	RO/LH	0
1.[3]	Auto-Negotiation Ability	1= auto-negotiation capable. (permanently =1) 0=Without auto-negotiation capability.	RO	1
1.[2]	Link Status	1=Link has never failed since previous read. 0=Link has failed since previous read. If link fails, this bit will be set to 0 until bit is read.	RO/LL	0
1.[1]	Jabber Detect	1=Jabber detected. 0=No Jabber detected. The jabber function is disabled in 100Base-X mode. Jabber is supported only in 10Base-T mode. Jabber occurs when a predefined excessive long packet is detected for 10Base-T. When the duration of TXEN exceeds the jabber timer (21ms), the transmit and loopback functions will be disabled and the COL LED starts blinking. After TXEN goes low for more than 500 ms, the transmitter will be re-enabled and the COL LED stops blinking.	RO/LH	0
1.[0]	Extended Capability	1=Extended register capable. 0=Not extended register capable. (permanently =1)	RO	1

4.8.5 Register2 : PHY Identifier 1 Register

Reg.bit	Name	Description	Mode	Default
2.[15:0]	OUI	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively.	RO	0243h

4.8.6 Register3 : PHY Identifier 2 Register

Reg.bit	Name	Description	Mode	Default
3.[15:10]	OUI	Assigned to the 19th through 24th bits of the OUI.	RO	000011b
3.[9:4]	Model Number	Manufacturer's model number 18h.	RO	010000 b
3.[3:0]	Revision Number	Manufacturer's revision number 00.	RO	0000b

4.8.7 Register4 : Auto-Negotiation Advertisement Register

Reg.bit	Name	Description	Mode	Default
4.[15]	Next Page	0=Next Page disabled. (Permanently =0)	RO	0
4.[14]	Reserved		RO	0
4.[13]	Remote Fault	1=Advertises that PHY has detected a remote fault. 0=No remote fault detected.	RW	0
4.[12]	Reserved		RO	0
4[11]	Asymmetric Pause	1=Advertises that PHY support asymmetric pause operation. 0=Not support asymmetric pause operation.	RW	0
4.[10]	Pause	1=Advertises that PHY has flow control capability. 0=Without flow control capability. **In 100FX, this bit is set by FX_PAUSE upon reset.**	TP_PAUSE Or FX_PAUSE	1
4.[9]	100Base-T4	Technology not supported. (Permanently =0)	RO	0
4.[8]	100Base-TX-FD	1=100Base-TX full duplex capable. 0=Not 100Base-TX full duplex capable.	RW	1
4.[7]	100Base-TX	1=100Base-TX half duplex capable. 0=Not 100Base-TX half duplex capable.	RW	1
4.[6]	10Base-T-FD	1=10Base-TX full duplex capable. 0=Not 10Base-TX full duplex capable.	RW	1
4.[5]	10Base-T	1=10Base-TX half duplex capable. 0=Not 10Base-TX half duplex capable.	RW	1
4.[4:0]	Selector Field	[00001]=IEEE802.3	RO	00001

4.8.8 Register5 : Auto-Negotiation Link Partner Ability Register

Reg.bit	Name	Description	Mode	Default
5.[15]	Next Page	1=Link partner desires Next Page transfer. 0=Link partner does not desire Next Page transfer.	RO	0
5.[14]	Acknowledge	1=Link Partner acknowledges reception of FLP words. 0=Not acknowledged by Link Partner.	RO	0
5.[13]	Remote Fault	1=Remote Fault indicated by Link Partner. 0=No remote fault indicated by Link Partner.	RO	0
5.[12]	Reserved		RO	0
5.[11]	Asymmetric Pause	1=Link partner support asymmetric pause operation. 0=Link partner not support symmetric operation. When the auto-negotiation is disabled, this bit is set to 1. After parallel detection, this bit is set to 1.	RO	0
5.[10]	Pause	1=Flow control supported by Link Partner. 0=No flow control supported by Link Partner. When the auto-negotiation is disabled, this bit is set to 1. After parallel detection, this bit is set to 1. **When in 100FX, this bit is set by FX_PAUSE or SMI.**.	RO	0
5.[9]	100Base-T4	1=100Base-T4 supported by Link Partner. 0=100Base-T4 not supported by Link Partner.	RO	0
5.[8]	100Base-TX-FD	1=100Base-TX full duplex supported by Link Partner. 0=100Base-TX full duplex not supported by Link Partner. For 100FX mode, this bit is set when Reg.0.[8]=1. When the auto-negotiation is disabled, this bit is set when Reg.0.[13]=1 and Reg.0.[8]=1.	RO	0
5.[7]	100Base-TX	1=100Base-TX half duplex supported by Link Partner. 0=100Base-TX half duplex not supported by Link Partner. For 100FX mode, this bit is set when Reg.0.[8]=0. When the auto-negotiation is disabled, this bit is set when Reg.0.[13]=1 and Reg.0.[8]=0. After parallel detection, this bit is set when the result of auto-negotiation is 100BASE-TX.	RO	0
5.[6]	10Base-T-FD	1=10Base-TX full duplex supported by Link Partner. 0=10Base-TX full duplex not supported by Link Partner. When the auto-negotiation is disabled, this bit is set when Reg.0.[13]=0 and Reg.0.[8]=1.	RO	0
5.[5]	10Base-T	1=10Base-TX half duplex supported by Link Partner. 0=10Base-TX half duplex not supported by Link Partner. When the auto-negotiation disabled, this bit is set when Reg.0.[13]=0,and Reg.0.[8]=0. After parallel detection, this bit is set when the result of auto-negotiation is 10BASE-TX.	RO	0
5.[4:0]	Selector Field	[00001]=IEEE802.3	RO	00001

4.8.9 Register6 : Auto-Negotiation Expansion Register

Reg.bit	Name	Description	Mode	Default
6.[15:5]	Reserved		RO	0
6.[4]	Parallel Detection Fault	1=A fault has been detected via the Parallel Detection function. 0=A fault has not been detected via the Parallel Detection function.	RO/LH	0
6.[3]	Link Partner Next Page Able	1= Link Partner is Next Page able. 0= Link Partner is not Next Page able. (permanently=0)	RO	0
6.[2]	Local Next Page Able	1= IP210T is Next Page able. 0= IP210T is not Next Page able.	RO	0
6.[1]	Page Received	1= A New Page has been received. 0= A New Page has not been received.	RO/LH	0
6.[0]	Link Partner Auto-Negotiation Able	If Nway is enabled, this bit means: 1= Link Partner is Auto-Negotiation able. 0= Link Partner is not Auto-Negotiation able.	0 (Nway) or 1 (100FX)	0

5 Register Description

5.1 Register Address Mapping

Address	Register
0x8000	Chip Configure Register_0
0x8001	Chip Configure Register_1
0x8002	CPU Control Register
0x8003	Status Register
0x8004	Interrupt Enable Register
0x8005	SW Reset Register
0x8006	Mirror Address Register
0x800f	**Timer Counter Register latch enable**
0x8010	**Timer Counter Register_0** (LSB)
0x8011	**Timer Counter Register_1**
0x8012	**Timer Counter Register_2**
0x8013	**Timer Counter Register_3** (MSB)
0x8014	PAD Control Register
0x8015	PHY Address Register
0x8100	**MAC_Control_Register_0**
0x8101	**MAC_Control_Register_1**
0x8102	**MAC_Control_Register_2**
0x8103	**Pause-On-Threshold_Register**
0x8104	**Pause-Off-Threshold_Register**
0x8110	TX Descriptor 0_0 - **TX_buffer_pointer_L**
0x8111	TX Descriptor 0_1 - **TX_buffer_pointer_H**
0x8112	TX Descriptor 0_2 - **Tx_Pkt_Length_L**
0x8113	TX Descriptor 0_3 - **Control_flag and Tx_Pkt_Length_H**
0x8114	TX Descriptor 1_0 - **TX_buffer_pointer_L**
0x8115	TX Descriptor 1_1 - **TX_buffer_pointer_H**
0x8116	TX Descriptor 1_2 - **Tx_Pkt_Length_L**
0x8117	TX Descriptor 1_3 - **Control_flag and Tx_Pkt_Length_H**
0x8118	TX Descriptor 2_0 - **TX_buffer_pointer_L**
0x8119	TX Descriptor 2_1 - **TX_buffer_pointer_H**
0x811a	TX Descriptor 2_2 - **Tx_Pkt_Length_L**
0x811b	TX Descriptor 2_3 - **Control_flag and Tx_Pkt_Length_H**
0x811c	TX Descriptor 3_0 - **TX_buffer_pointer_L**
0x811d	TX Descriptor 3_1 - **TX_buffer_pointer_H**
0x811e	TX Descriptor 3_2 - **Tx_Pkt_Length_L**
0x811f	TX Descriptor 3_3 - **Control_flag and Tx_Pkt_Length_H**
0x8130	RX_Buffer_Start_Address
0x8131	RX_Buffer_Read_Pointer_L

Address	Register
0x8132	RX_Buffer_Read_Pointer_H
0x8133	RX_Buffer_Write_Pointer_L
0x8134	RX_Buffer_Write_Pointer_H
0x8135	RX_Filter_Registers_0
0x8136	RX_Filter_Registers_1
0x8137	Ether_Type_Start_Offset_Register
0x8138	Special_Source_Port_Tag_Type_Register_L
0x8139	Special_Source_Port_Tag_Type_Register_H
0x8200	**DMA_Command_Register**
0x8201	**DMA_Source_Address_Register_L**
0x8202	**DMA_Source_Address_Register_H**
0x8203	**DMA_Destination_Address_Register_L**
0x8204	**DMA_Destination _Address_Register_H**
0x8205	**DMA_Length_Register_L**
0x8206	**DMA_Length_Register_H**
0x8207	CRC_Result_Register_0
0x8208	CRC_Result_Register_1
0x8209	CRC_Result_Register_2
0x820a	CRC_Result_Register_3
0x820b	Preset_CRC_Value_Register
0x8310	EEPROM_Data_Register
0x8311	EEPROM_Addresss_Register
0x8312	EEPROM_ID_Register
0x8313	EEPROM_**Command_Register**
0x8314	EEPROM_**Control_Register**
0x8320	MD_Control_reg
0x8321	MD_PhyAddress
0x8322	MD_RegAddress
0x8323	MD_Data_Low
0x8324	MD_Data_High
0x8330	My MAC Address Byte 0 (LSB)
0x8331	My MAC Address Byte 1
0x8332	My MAC Address Byte 2
0x8333	My MAC Address Byte 3
0x8334	My MAC Address Byte 4
0x8335	My MAC Address Byte 5 (MSB)
0x8336	My IPV4 Byte 0 (LSB)

Address	Register
0x8337	My IPV4 Byte 1
0x8338	My IPV4 Byte 2
0x8339	My IPV4 Byte 3 (MSB)
0x8350	RMT_MAC Byte 0 (LSB)
0x8351	RMT_MAC Byte 1
0x8352	RMT_MAC Byte 2
0x8353	RMT_MAC Byte 3
0x8354	RMT_MAC Byte 4
0x8355	RMT_MAC Byte 5 (MSB)
0x8356	RMT IPV4 Byte 0 (LSB)
0x8357	RMT IPV4 Byte 1
0x8358	RMT IPV4 Byte 2
0x8359	RMT IPV4 Byte 3 (MSB)
0x8370	ADC Control Register
0x8371	ADC Result Register L
0x8372	ADC Result Register H
0x8400	Chip ID LO
0x8401	Chip ID HI
0x8402	Chip Revision
0x8800	UART Receive Buffer (RO)
0x8801	UART_Transmit Buffer (WO)
0x8802	UART_Interrupt Enable
0x8803	UART_Interrupt Identification (RO)
0x8804	UART_FIFO Control
0x8805	UART_Line Control Register
0x8806	UART_Modem Control
0x8807	UART_Line Status(RO)
0x8808	UART_Modem Status(RO)
0x8809	UART_TX FIFO Status (RO)
0x880a	UART_RX FIFO Status (RO)
0x880b	UART_Clock Divisor Registers_L **(when the 7th (DLAB) bit of the Line Control Register is set to '1')**
0x880c	UART_Clock Divisor Registers_H **(when the 7th (DLAB) bit of the Line Control Register is set to '1')**

5.2 Register Descriptions

Chip Configure Register_0 (0x8000)

Bit	Name	Access	Description	Default
0	Reserved	R		0
1	Reserved	R		0
3-2	Reserved	RW	Reserved. Do not change this configuration.	01
4	Reserved	RW	Reserved. Do not change this configuration.	0
5	Mirror_En	RW	Redirect Code Bus to first 8K or 16K SRAM and the start address is defined in MirrorAddress register. 1: Enable redirect 0: Code Bus to OTP or Flash (defined in bit 0)	0
6	Link_led_at_clk25_En	RW	1: Enable Link LED output 0: CLK25 output	0
7	Reserved	RW		0

Chip Configure Register_1 (0x8001)

Bit	Name	Access	Description	Default
0	Reserved	RW		0
1	HSP_UART_En	RW	1: High Speed UART enable 0: GPIO2	0
2	Reserved	RW		0
3	Reserved	RW		0
4	P3_I2C_En	RW	1: P3 I2C interface enable (P3.7 = SCL, P3.6 =SDA) 0: GPIO3 bit6 & bit7	0
5	Reserved	RW		0
6	Reserved	RO		X
7	Reserved	RO		X

CPU Control Register (0x8002)

Bit	Name	Access	Description	Default
0	Write_En	RW	This bit is used to change this register bit[7:1] from RO to RW 1 – Enable Write Access to bit[7:1] 0 – RO to bit[7:1]	0
4-1	OTP_WaitState	RW	Default is 0x7	0111
7-5	Reserved			

Status register (0x8003)

Bit	Name	Access	Description	Default
0	RX_Packet_Done	RC	H/W sets 1 to inform CPU that one or more packets are received in RX buffer.	0
1	TX_Packet_Done	RC	H/W sets 1 to inform CPU that TX packet is done.	0
2	DMA_Access_Done	RC	H/W sets 1 to indicate that DMA is done.	0
3	Timer_Counter_overflow	RC	H/W sets 1 to indicate that timer counter overflow.	0
4	HighSpeed_UART_Status_change	RC	H/W sets 1 to indicate that High Speed UART Status Changed	0
5	ADC_Done	RC	H/W sets 1 to inform CPU that ADC is done	0
6	PHY_Status_change	RC	H/W sets 1 to indicate that PHY Status Changed	0
7	Reserved	-	-	

Interrupt Enable register (0x8004)

Bit	Name	Access	Description	Default
0	RX_Packet_Done_Enable	RW	1: enable RX_Packet_Done interrupt 0: disable RX_Packet_Done interrupt	0
1	TX_Packet_Done_Enable	RW	1: enable TX_Packet_Done interrupt 0: disable TX_Packet_Done interrupt	0
2	DMA_Access_Don_Enable	RW	1: enable DMA_Access_Done interrupt 0: disable DMA_Access_Done interrupt	0
3	Timer_Counter_overflow_Enable	RW	1: enable Timer_Counter_overflow interrupt 0: disable Timer_Counter_overflow interrupt	0
4	HighSpeed_UART_Status_Enable	RW	1: enable HighSpeed_UR_Status_change interrupt 0: disable HighSpeed_UR_Status_change interrupt	0
5	ADC_Done_Enable		1: enable ADC_Done interrupt 0: disable ADC_Done interrupt	0
6	PHY_Status_Enable		1: enable PHY_Status_change interrupt 0: disable PHY_Status_change interrupt	0
7	Reserved	-	-	

SW Reset Register (0x8005)

Bit	Name	Access	Description	Default
0	**Reset**	RW	This bit is used to reset all the peripherals and registers except ChipConfig, CPU Control register and bit0/1 of MAC Control register 0 and CPU 1. Write 0 to this bit is ignored by IP210T. 2. Write 1 to this bit will cause IP210T doing reset to all peripherals. This bit will be auto-cleared when reset is done.	0
7-1	Reserved			

Mirror Address Register (0x8006)

Bit	Name	Access	Description	Default
7-0	**Mirror Start Address**	RW	This register defines the starting address bit[15:8] of SRAM code when 8K_Mirror_En=1 or 16K_Mirror_En=1	00h

Timer Counter Register latch enable (0x800f)

Bit	Name	Access	Description	Default
0	Timer Count latch enable	WO	1: Latch Current Timer Counter Register. 0: No action	0
7-1	Reserved			

Timer Counter Register 4 bytes (0x8013[MSB] ~ 0x8010[LSB])

Bit	Name	Access	Description	Default
31-0	Timer Count	RW	Timer Counter Register is a 32-bit counter and is incremented upon the overflow of Timer2 (TF2). User can set Timer2 to determine the overflow intervals. Its value wraps around to 0x00 00 00 00 at Timer2's overflow while its previous value is 0xff ff ff ff.	00 00 00 00h

PAD Control Register (0x8014)

Bit	Name	Access	Description	Default
1-0	IO_Driving	RW	00: 2 mA 01: 4 mA 10: 8 mA 11 12 mA	01
2	IO_Speed	RW	0: Normal 1: Fast	0
7-3	Reserved			

PHY Address Register (0x8015)

Bit	Name	Access	Description	Default
4-0	PHY Address	RW	1f	11111
7-5	Reserved			0

MAC_Control_register_0 (0x8100)

Bit	Name	Access	Description	Default
0	Speed100	RW	Speed setting bit (This bit is for RMII only): 1-100Mbps 0-10MbpsDriver use it to force the speed of MAC.	1
1	Duplex_F	RW	Duplex setting bit: 1- Full duplex 0- Half duplex, Driver use it to force the duplex mode of MAC.	1
2	TX_Enable	RW	Enable Transmission function of MAC: 0- disable 1- enable	0
3	RX_Enable	RW	Enable Receive function of MAC: 0- disable 1- enable	0
4	FlowControl_Enable	RW	1: Enable Flow Control function of MAC. In full duplex mode, MAC will act as follows: a.MAC will issue Pause frame with 0xFFFF when used RX buffer is over Pause-On-Threshold and continue to issue Pause frame with 0xFFFF only if remote node keeps on transmitting. b. MAC will send Pause frame with 0x0000 when used RX buffer is under Pause-Off-Threshold. c. MAC will stop transmitting if MAC receive a Pause frame with time > 0 and resume TX if MAC received a Pause frame with 0x0000 frame or timeout which is set by Pause frame with time > 0. In half duplex mode, MAC will do nothing. 0: Disable FlowControl	0
5	Boff_16_off	RW	This bit will disable maximum 16-retry limit and do infinite retry when the bit is set to 1.	0
6	LoopBack	RW	Enable MII-Internal-LoopBack when the bit is set to 1.	0
7	MaxFrameLen	RW	This bit sets the maximum receive packet length. 1- 1536 bytes 0- 1522 bytes	1

MAC_Control_register_1 (0x8101)

Bit	Name	Access	Description	Default
0	FCS-append-disable	RW	0: TXMAC auto-calculates and auto-appends 4 bytes CRC at the end of packet. 1: TXMAC do NOT append 4 bytes CRC at the end of packet.	0
1	FCS-receive-enable	RW	0: RXMAC do NOT receive 4 bytes CRC into RX-Buffer. 1: RXMAC receive 4 bytes CRC into RX-Buffer.	0
2	SourcePortTagInserted_En	RW	0: RXMAC will not check if there is a SourcePortTag inserted right after SA. RXMAC treats the word right after SA as an EtherType. 1: RXMAC will check if there is a SourcePortTag, which has type value same as the SourcePortTagType register, inserted right after SA. If yes, RXMAC will skip 4 bytes from SA and treat the subsequent word as EtherType. If not, EtherType is considered right after SA. If SourcePortTagInserted_En="1" and first type != 0x9126(or SourcePortTag type Register), then drop the frame.	0
4-3	IGMP_Mode_En	RW	00 or 11: RXMAC will treat IGMP frame as normal frame and filter the frame according to RX Filter rules. 01: RXMAC will receive in IGMP frame (IP frame with IP protocol=2) with DA=Multicast address of range 01-00-5E-00-00-00~~01-00-5E-7F-FF-FF and set the frame type to 1011b (IGMP frame). 10: RXMAC will receive in IGMP frame (IP frame with IP protocol=2) without DA constraint – Multicast or Unicast and set the frame type in RX buffer to 1011b (IGMP frame) **IGMP frame is an IP frame with IP protocol=2	00
5	Rx_8021X_En	RW	0: RXMAC will not receive frame with Multicast DA = 01-80-C2-00-00-03 1: RXMAC will receive 802.1X frame with DA=01-80-C2-00-00-03 and set the frame type in RX buffer to 1100b (802.1X frame)	0
6	Reserved			
7	Reset_TXMAC	RW	When this bit is written to 1, the system will reset TXMAC and clear following registers.	0

			1. Tx_Enable (0x8100[2]) 2. Boff_16_off (0x8100[5]) 3. FCS-append-disable (0x8101[0]) 4. Tx Descriptors (0x8110~0x811f) 5. DMA_CMD_mode(0x8200[2:0]) P.S. when 0x 8200[2:0]=101 or 110 6. CRC_Result_Register (0x8207~0x820a) This bit will be self-cleared after TXMAC reset is done. Writing a "0" to this bit is ignored by H/W.	

MAC_Control_register_2 (0x8102)

Bit	Name	Access	Description	Default
0	IP_Checksum_Insp	RW	IP Checksum inspection function 1: enable 0: disable	1
1	TCP_Checksum_Insp	RW	TCP Checksum inspection function 1: IP210T drops the incoming packet if its TCP Checksum has errors 0: disable	1
2	UDP_Checksum_Insp	RW	UDP Checksum inspection function 1: IP210T drops the incoming packet if its UDP Checksum has errors 0: disable	1
3	ICMP_Checksum_Insp	RW	ICMP Checksum inspection function 1: IP210T drops the incoming packet if its ICMP Checksum has errors 0: disable	1
7-4	Reserved	-		

Pause -On-Threshold_register (0x8103)

Bit	Name	Access	Description	Default
7-0	Pause -On-Threshold	RW	(Unit is 256 bytes) Pause-On-Threshold[7:0] = 0x30= 8'd48 ---> 48*256bytes = 12K bytes	30h

Pause -Off-Threshold_register (0x8104)

Bit	Name	Access	Description	Default
7-0	Pause -Off-Threshold	RW	(Unit is 256 bytes) Pause-Off-Threshold[7:0] = 0x18= 8'd24 ---> 24*256bytes = 6K bytes	18h

TX Descriptor 0_0 - TX_buffer_pointer_L (0x8110)

Bit	Name	Access	Description	Default
7-0	TX_Buffer_Ptr_L	RW	This field defines TX buffer pointer bit [7:0]	00h

TX Descriptor 0_1 - TX_buffer_pointer_H (0x8111)

Bit	Name	Access	Description	Default
7-0	TX_Buffer_Ptr_H	RW	This field defines TX buffer pointer bit [13:8]	00h

TX Descriptor 0_2 - Tx_Pkt_Length_L (0x8112)

Bit	Name	Access	Description	Default
7-0	TX_Len_L	RW	This field defines TX frame length bit [7:0]	00h

TX Descriptor 0_3 - Control_flag and Tx_Pkt_Length_H (0x8113)

Bit	Name	Access	Description	Default
2-0	TX_Len_H	RW	This field defines TX frame length bit [10:8]	000
5-3	Checksum_Packet_Type	RW	This field enable packet by packet MAC checksum insertion action: 000- No IP checksum insertion requirement 001- IP/TCP IPv4 checksum insertion 010- IP/UDP IPv4 checksum insertion 011- IP/ICMP IPv4 checksum insertion	000
6	TX_Error	RO	This bit will be auto-cleared when bit 7, Start_TX, is written to “1”. This bit is valid only when bit 7, Start_TX, is written to “0”. 0: TX no error 1: TX error such as TxUnderrun, MaxCollision, LateCollision, etc.	0
7	Start_TX	RW	The TX MAC will start to send this packet when this bit is set to “1”. It’s auto-cleared when TX is done. Writing this bit to “0” will be ignored by H/W.	0

TX Descriptor 1_0 ~ TX Descriptor 1_3 (0x8114 ~ 0x8117)
TX Descriptor 2_0 ~ TX Descriptor 2_3 (0x8118 ~ 0x811b)
TX Descriptor 3_0 ~ TX Descriptor 3_3 (0x811c ~ 0x811f)

Rx-Buffer-Start-Address (0x8130)

Bit	Name	Access	Description	Default
7-0	Rx-Buffer-Start-Address	RW	This byte defines the high byte of RX Buffer Start address in internal RAM. The low byte of RX Buffer Start address is always 00h	40h

RX_Buffer_Read_Pointer_L (0x8131)

Bit	Name	Access	Description	Default
7-0	Rx-Buffer-Read-Pointer-L	RW	Rx-Buffer-Read-Pointer Low Byte. It is maintained by S/W to store the address of the first unread received frame.	00h

RX_Buffer_Read_Pointer_H (0x8132)

Bit	Name	Access	Description	Default
7-0	Rx-Buffer-Read-Pointer-H	RW	Rx-Buffer-Read-Pointer High Byte. It is maintained by S/W to store the address of the first unread received frame.	40h

RX_Buffer_Write_Pointer_L (0x8133)

Bit	Name	Access	Description	Default
7-0	Rx-Buffer-Write-Pointer-L	RW	Rx-Buffer-Write-Pointer Low Byte. It is maintained by H/W to store the address of the incoming frame.	00h

RX_Buffer_Write_Pointer_H (0x8134)

Bit	Name	Access	Description	Default
7-0	Rx-Buffer-Write-Pointer-H	RW	Rx-Buffer-Write-Pointer High Byte. It is maintained by H/W to store the address of the incoming frame.	40h

RX_Filter_registers_0 (0x8135)

Bit	Name	Access	Description	Default
0	Rx_My_Mac_En	RW	1: MAC will filter out the unicast frame except its DA equal to MY_MAC_ADDRESS. 0: MAC will filter out all unicast frames. Pause frame will be recognized by the MAC according to the state of Rx_Pause_En.	1
1	Rx_Mcst_En	RW	1: MAC will receive all multicast frame except BPDU, PAUSE, IGMP and 802.1X frame 0: MAC will filter out all multicast frame except BPDU, PAUSE, IGMP and 802.1X frame. BPDU and PAUSE frame filters are defined in bit 4 and bit5. IGMP and 802.1X are defined in MAC_Control_register_1, Bit-4-3 and Bit-5. **Note:** DA of BPDU : 01-80-C2-00-00-00 DA of PAUSE : 01-80-C2-00-00-01 DA of IGMP: 01-00-5E-00-00-00 ~ 01-00-5E-7F-FF-FF DA of 802.1X: 01-80-C2-00-00-03	0
2	Rx_Bcast_En	RW	1: MAC will receive Broadcast frame 0: MAC will filter out Broadcast frame except Broadcast ARP and Broadcast RARP frame.	0
3	Rx_All_En	RW	1: enable MAC to receive all good frame except Pause packet 0: MAC will receive frame by checking the setting of the other bits of RX_Filter_registers_0 and RX_Filter_registers_1.	0
4	Rx_Bpdu_En	RW	1: MAC will receive BPDU packet 0: MAC will filter out BPDU packet BPDU is a frame with DA=01-80-C2-00-00-00	0
5	Rx_Pause_En	RW	1: if MAC_Control_register_0.FlowControl_Enable=0, MAC will receive Pause packet. 0: MAC will filter out Pause packet. Pause packet is a frame with DA =01-80-C2-00-00-01 or My_MAC_Address Type = 0x8808 OP Code= 0x0001	0

6	Rx_Remote_Mac	RW	MAC will receive only the frame with SA=Remote_MAC_Address when this bit set 1. This bit is used to lock remote node's MAC Address.	0
7	Rx_CRCErr_En	RW	0: MAC will filter out CRC error frame. 1: Enable MAC to receive CRC error frame.	0

RX_Filter_registers_1 (0x8136)

Bit	Name	Access	Description	Default
0	Rx_MyIP_En	RW	MAC will receive only the frame with Destination IP = My_IP when this bit is set 1.	1
1	Rx_RemoteIP_En	RW	MAC will receive only the frame with Source IP = Remote_IP when this bit is set 1.	0
3-2	Rx_IP_Type_En	RW	00 - Receive all EtherType frame except the setting defined in RX_Filter_register_0.Rx_Pause_En 01- Receive EtherType only IPv4(0x800), ARP(0x806), RARP(0x8035). *Notice: (a) If the EtherType is 0x0800 but the subsequent byte is not equal to IPV4 version, the MAC will drop the frame. (b) If the EtherType is 0x8100 (VLAN packet), No matter the setting of Rx_IP_Type_En value, The RXMAC will always skip 4 bytes VLAN tagging and treat the subsequent word as EtherType.	01
7-4	Reserved	-	-	

Ether_Type_Start_Offset_Register (0x8137)

Bit	Name	Access	Description	Default
7-0	Ether_Type_Start_Offset	RW	Define the Byte-Offset of EtherType Field from SA-Field of receiving packet The default value is 0. It means EtherType field is right after SA field in the receiving frame. Ex: If Ether_Type_Start_Offset= 0x6, the EtherType field will be located at Byte 18/19 in the receiving frame start the byte count from 0.	00h

Special_Source_Port_Tag_Type_Register_L (0x8138)

Bit	Name	Access	Description	Default
7-0	Special_Source_Port_Tag_ Type_Register_L	RW	Source Port Tag Type Value low byte	26h

Special_Source_Port_Tag_Type_Register_H (0x8139)

Bit	Name	Access	Description	Default
7-0	Special_Source_Port_Tag_ Type_Register_H	RW	Source Port Tag Type Value high byte	91h

DMA_Command_Register (0x8200)

Bit	Name	Access	Description	Default
2-0	CMD_mode	RW	000-No DMA operating or DMA done. 001-Internal Data to Internal Data transfer. 010- Reserved 011- Reserved 100-OTP ROM to Internal Data transfer. 101-Interanl data to CRC32 generation. The CRC32 result will be calculated by IP210T and be stored in CRC_Result_register (0-3). 110-Interanl data to checksum generation and insert into checksum fields in IP packet memory pointed by DMA_Source_Address.	000
3	Reserved	-	-	
7-4	Packet_Type	RW	Indicates the packet type when using DMA to calculate the packet checksum (CMD_mode=110): 0000- no checksum generation needed 0001- IP and TCP (IPv4) 0010- IP and UDP (IPv4) 0011- IP and ICMP (IPv4) Others- no checksum generation needed. Note: The calculated result is stored in CRC_Result_Register.	0000

DMA_Source_Address_Register_L (0x8201)

Bit	Name	Access	Description	Default
7-0	DMA_Source_Address_L	RW	DMA source address low byte	00h

DMA_Source_Address_Register_H (0x8202)

Bit	Name	Access	Description	Default
7-0	DMA_Source_Address_H	RW	DMA source address high byte	00h

DMA_Destination_Address_Register_L (0x8203)

Bit	Name	Access	Description	Default
7-0	DMA_Destination_Address_L	RW	DMA Destination address low byte	00h

DMA_Destination_Address_Register_H (0x8204)

Bit	Name	Access	Description	Default
7-0	DMA_Destination_Address_H	RW	DMA Destination address high byte	00h

DMA_Length_Register_L (0x8205)

Bit	Name	Access	Description	Default
7-0	DMA_Length_L	RW	It specifies the low byte of the length of data for IP checksum or CRC32 calculation. The maximum value of DMA_length is 2047.	00h

DMA_Length_Register_H (0x8206)

Bit	Name	Access	Description	Default
7-0	DMA_Length_H	RW	It specifies the high byte of the length of data for IP checksum or CRC32 calculation. The maximum value of DMA_length is 2047.	00h

CRC_Result_Register(3~0) (0x820a ~ 0x8207)

Bit	Name	Access	Description	Default
31-0	CRC_Result	RW	These registers store the calculatedresult of CRC32. There are two conditions to set the register to 0xFFFFFFFF: (a) Power on reset (b) Write 1 to Preset_CRC_Value_Register	FF FF FF FFh

Preset_CRC_Value_Register (0x820b)

Bit	Name	Access	Description	Default
0	Preset_CRC_Value	RW	Setting this bit to 1 will trigger HW_CRC to preset CRC_Result_register(0-3) to 0xFFFFFFFF. This bit will be self-cleared when HW-CRC has done the reset of CRC_Result_register. Writing 0 to this bit is ignored by HW_CRC.	0
7-1	Reserved			

EEPROM_Data_Register (0x8310)

Bit	Name	Access	Description	Default
7-0	EEPROM_Data	RW	It stores the data to be written to/read from EEPROM.	00h

EEPROM_Addresss_Register (0x8311)

Bit	Name	Access	Description	Default
7-0	EEPROM_Addr	RW	It defines the address of EEPROM.	00h

EEPROM_ID_Register (0x8312)

Bit	Name	Access	Description	Default
2-0	EEPROM_ID	RW	It defines EEPROM ID or EEPROM address high bits for EEPROM with size over 256 bytes such as 24C16/24C08/24C04. The ID bit(s) should be filled with 0. For example: 24C16 – bit[2:0] define address[10:8] 24C08 – bit[2] is ID[A2], bit[1:0] define address[9:8]	000
7-3	Reserved			

	Bit 2	Bit 1	Bit 0
24C01	ID	ID	ID
24C02	ID	ID	ID
24C04	ID	ID	Addr[8]
24C08	ID	Addr[9]	Addr[8]
24C16	Addr[10]	Addr[9]	Addr[8]

EEPROM_Command_Register (0x8313)

Bit	Name	Access	Description	Default
4-0	Byte_count	RW	Define the access size. The access size is (Byte_count+1) bytes. In EEPROM writing operation, if the access size over a page (16bytes or 8 bytes which is dependent on EEPROM type), the oversize part will be written to the address starts from the beginning of the page and overwrite the previous data.	00000
5	RW_op	RW	Define the operation: 0- Write 1- Read	0
6	Abort	RW	If this bit=1, the H/W abort the access operation defined by RW_op. This bit will be auto-cleared by H/W after a read or write operation.	0
7	Next	RW	If this bit=1, the H/W is available for the next read or write operation. This bit will be auto-cleared by H/W after a read or write operation.	0

EEPROM_Control_ Register (0x8314)

Bit	Name	Access	Description	Default
0	EE_Clk_Sel	RW	0: EEPROM clock rate is 58.9KHz, for normal usage. 1: Speed-up mode, EEPROM clock rate is 5.89MHz. This mode is used for test only.	0
7-1	Reserved		.	

MD_Control_reg (0x8320)

Bit	Name	Access	Description	Default
2-0	MDC_Clock_Select	RW	000 – 34ns 001 – 68ns 010 – 136ns 011 – 272ns 100 – 544ns(recommend) 101 – 1088ns 110 – 2176ns	000
3	Reserved			
4	RW_op	RW	1: for Read operation 0: for Write operation	0
5	Preamble_Disable	RW	0: Add preamble to the packet 1: Do not add the preamble to the packet.	0
6	Reserved			
7	Start	RW	Set 1 to start MDC/MDIO operation Auto-cleared when the operation is completed.	0

MD_PhyAddress (0x8321)

Bit	Name	Access	Description	Default
4-0	Phy Address	RW	Phy Address	00000
7-5	Reserved			

MD_RegAddress (0x8322)

Bit	Name	Access	Description	Default
4-0	Register Address	RW	Register Address	00000
7-5	Reserved			

MD_Data_Low (0x8323)

Bit	Name	Access	Description	Default
7-0	MD_Data_Low	RW	MD_Data[7:0]	00h

MD_Data_High (0x8324)

Bit	Name	Access	Description	Default
7-0	MD_Data_High	RW	MD_Data[15:8]	00h

My MAC Address 6 bytes (0x8335[MSB] ~ 0x8330[LSB])

Bit	Name	Access	Description	Default
47-0	My MAC Address	RW	My MAC Address [47:0]	00 00 00 00 00 00h

My IPv4 Address 4 bytes (0x8339[MSB] ~ 0x8336[LSB])

Bit	Name	Access	Description	Default
31-0	My IPv4 Address	RW	My IPv4 Address [31:0]	00 00 00 00h

Remote MAC Address 6 bytes (0x8355[MSB] ~ 0x8350[LSB])

Bit	Name	Access	Description	Default
47-0	Remote MAC Address	RW	Remote MAC Address [47:0]	00 00 00 00 00 00h

Remote IPv4 Address 4 bytes (0x8359[MSB] ~ 0x8356[LSB])

Bit	Name	Access	Description	Default
31-0	Remote IPv4 Address	RW	Remote IPv4 Address [31:0]	00 00 00 00h

ADC Control Register 0 (0x8370)

Bit	Name	Access	Description	Default
0	ADON	RW	A/D On bit 1 = A/D converter module is enabled and begin to calibrate 0 = A/D converter module is disabled	0
1	START	RW	A/D conversion status bit ADON = 1 : 1 = A/D conversion in progress 0 = A/D idle This bit will be auto-cleared when AD is done	0
3-2	VRS	RW	voltage reference select bits 0 0 vdda / vssa 0 1 External Vref+ / vssa 1 0 vdda / External Vref- 1 1 External Vref+ / External Vref-	00
6-4	PA	RW	Analog channel select bits 0 0 0 = channel 0 (P0) 0 0 1 = channel 1 (P1) 0 1 0 = Reserved 0 1 1 = Reserved 1 0 0 = Reserved 1 0 1 = Reserved 1 1 0 = Reserved 1 1 1 = Reserved	000
7	Calibrated	RW	Calibration done 1 = A/D converter module is calibrated 0 = A/D converter module is not calibrated	0

ADC Result Register L (0x8371)

Bit	Name	Access	Description	Default
7-0	ADC Result Register L	RW	ADC Result Register Low byte	00h

ADC Result Register H (0x8372)

Bit	Name	Access	Description	Default
7-0	ADC Result Register H	RW	ADC Result Register High byte	00h

Chip ID LO (0x8400)

Bit	Name	Access	Description	Default
7-0	Chip ID LO	RO	Chip ID Number Low byte	10h

Chip ID HI (0x8401)

Bit	Name	Access	Description	Default
7-0	Chip ID HI	RO	Chip ID Number high byte	02h

Chip Revision (0x8402)

Bit	Name	Access	Description	Default
7-0	Chip Revision	RO	Chip reversion Number	00h

UART_Receiver Buffer (0x8800)

Bit	Name	Access	Description	Default
7-0	UART_Receiver Buffer	RO	UART Receiver FIFO output.	00h

UART_Transmit Buffer (0x8801)

Bit	Name	Access	Description	Default
7-0	UART_Transmit Buffer	WO	UART Transmit FIFO input.	

Interrupt Enable Register IER (0x8802)

This register allows enabling and disabling interrupt generation by the UART

Bit	Name	Access	Description	Default
0	Received Data available interrupt	RW	'0' – disabled '1' – enabled	0
1	Transmitter Holding Register empty interrupt	RW	'0' – disabled '1' – enabled	0
2	Receiver Line Status Interrupt	RW	'0' – disabled '1' – enabled	0
3	Reserved	RW	Reserved. Should be logic '0'.	
4	Received Data Timeout interrupt	RW	'0' – disabled '1' – enabled	0
7-5	Reserved	RW	Reserved. Should be logic '0'.	

Interrupt Identification Register IIR (0x8803)

The IIR enables the programmer to retrieve the current highest priority pending interrupt.
Bit 0 indicates that an interrupt is pending when it's logic '0'. When it's '1' – no interrupt is pending.
The following table displays the list of possible interrupts along with the bits they enable, priority, and their source and reset control.

Bit 3	Bit 2	Bit 1	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	1	1	1st	Receiver Line Status	Parity, Overrun or Framing errors or Break Interrupt	Reading the Line Status Register
0	1	0	2nd	Receiver Data available	FIFO trigger level reached	FIFO drops below trigger level
1	1	0	2nd	Timeout Indication	There's at least 1 character in the FIFO but no character has been input to the FIFO or read from it for the last 4 Char times.	Reading from the FIFO (Receiver Buffer Register)
0	0	1	3rd	Transmitter Holding Register empty	Transmitter Holding Register Empty	Writing to the Transmitter Holding Register or reading IIR.

Bits 4 and 5: Logic '0'.
Bits 6 and 7: Logic '1'.
Default Value: 0xC1

FIFO Control Register FCR (0x8804)

The FCR allows the selection of the FIFO trigger level (the number of bytes in FIFO required to enable the Received Data Available interrupt). In addition, the FIFOs can be cleared using this register.

Bit	Name	Access	Description	Default
0	Clears the Receiver FIFO	RW	Writing a '1' to bit 1 clears the Receiver FIFO and resets its logic.	0
1	Clears the Transmitter FIFO	RW	Writing a '1' to bit 2 clears the Transmitter FIFO and resets its logic.	0
7-2	Receiver FIFO Interrupt trigger level	RW	Define the Receiver FIFO Interrupt trigger level[7:2], Interrupt trigger level[1:0] always equal to 2'b00 Ex : '000001' – 4 bytes '010000' –64 bytes	010000

Line Control Register LCR (0x8805)

The line control register allows the designer to define the specification of the asynchronous data communication used. A bit in the register also allows the access to the Divisor Latches, which define the baud rate. Reading from the register is allowed to check the current settings of the communication.

Bit	Name	Access	Description	Default
1-0	number of bits in each character	RW	Select number of bits in each character '00' – 5 bits '01' – 6 bits '10' – 7 bits '11' – 8 bits	11
2	number of generated stop bits	RW	Specify the number of generated stop bits '0' – 1 stop bit '1' – 1.5 stop bits for 5-bit character length selected; 2 bits for others. Note that the receiver always checks the first stop bit only.	0
3	Parity Enable	RW	'0' – No parity '1' – Parity bit is generated on each outgoing character and is checked on each incoming one.	0
4	Even Parity select	RW	'0' – Odd number of '1' is transmitted and checked in each word (data and parity combined). In other words, if the data has an even number of '1' in it, then the parity bit is '1'. '1' – Even number of '1' is transmitted in each word.	0
5	Stick Parity bit	RW	'0' – Stick Parity disabled '1' - If bits 3 and 4 are logic '1', the parity bit is transmitted and checked as logic '0'. If bit 3 is '1' and bit 4 is '0' then the parity bit is transmitted and checked as '1'.	0
6	Break Control bit	RW	'1' – the serial out is forced into logic '0' (break state). '0' – break is disabled (default)	0
7	Divisor Latch Access bit	RW	'1' – The UART_Clock Divisor Registers is accessible '0' – The UART_Clock Divisor Registers can't be accessed (Please refer to UART _Clock Divisor Registers for detail)	0

Modem Control Register MCR (0x8806)

The modem control register allows transferring control signals to a modem connected to the UART.

Bit	Name	Access	Description	Default
0	Data Terminal Ready (DTR) signal control	RW	'0' – DTR is '0' '1' – DTR is '1'	0
1	Request To Send (RTS) signal control	RW	'0' – RTS is '0' '1' – RTS is '1'	0
2	Out1	RW	In loopback mode, connected Ring Indicator (RI) signal input.	0
3	Out2	RW	In loopback mode, connected to Data Carrier Detect (DCD) input.	0
4	Loopback mode	RW	'0' – normal operation '1' – loopback mode. When in loopback mode, the Serial Output Signal (STX_PAD_O) is set to logic '1'. The signal of the transmitter shift register is internally connected to the input of the receiver shift register. The following connections are made: DTR ➔ DSR RTS ➔ CTS Out1 ➔ RI Out2 ➔ DCD	0
5	HW_RTS_Stop_TX_En	RW	'0' – normal operation '1' –When RTS = 1, the transmitter will stop sending other characters after sending current character.	0
6	HW_TX_Disable	RW	'0' – normal operation '1' –the transmitter will stop sending other characters after sending current character	0
7	HW_FlowControl_En	RW	'0' – normal operation '1' – enable HW Flow Control, by RTS & CTS Rx part: when RXFIFO content characters higher than RXFIFO interrupt level (0x8804), the RTS will be pulled high; otherwise RTS will be pulled low. Tx part: If CTS is pulled high, the transmitter will stop sending other characters after sending current character.	0

Line Status Register LSR (0x8807)

Bit	Name	Access	Description	Default
0	Data Ready (DR) indicator	RO	'0' – No characters in the FIFO '1' – At least one character has been received in the FIFO.	0
1	Overrun Error (OE) indicator	RO	'1' – If the FIFO is full and another character has been received in the receiver shift register. If another character is about to arrive, it will overwrite the data in the shift register but the FIFO will remain intact. The bit is cleared upon reading from the register. IP210T generates Receiver Line Status interrupt when detecting Overrun Error. '0' – No overrun state	0
2	Parity Error (PE) indicator	RO	'1' – At least one character in FIFO has been detected as having parity error. When this bit is read as '1', all characters in FIFO should be read and dropped. The bit is cleared upon a read from the register. IP210T generates Receiver Line Status interrupt when detecting Parity Error. '0' – No parity error in the current character	0
3	Framing Error (FE) indicator	RO	'1' – The received character at the top of the FIFO did not have a valid stop bit. Of course, generally, it might be that all the following data is corrupt. The bit is cleared upon reading from the register. IP210T generates Receiver Line Status interrupt when detecting Framing Error. '0' – No framing error in the current character	0
4	Break Interrupt (BI) indicator	RO	'1' –A break condition has been reached in the current character. The break occurs when the line is held in logic 0 for a time of one character (start bit + data + parity + stop bit). In that case, one zero character enters the FIFO and the UART waits for a valid start bit to receive next character. The bit is cleared upon reading from the register. IP210T generates Receiver Line Status interrupt when detecting a Break Interrupt. '0' – No break condition in the current character	0
5	Transmit FIFO is empty	RO	'1' –. IP210T generates Transmitter Holding Register Empty interrupt when the transmitter FIFO is empty. The bit is cleared when data is written to the transmitter FIFO. '0' – Otherwise	1
6	Transmitter Empty indicator	RO	'1' – Both the transmitter FIFO and transmitter shift register are empty. The bit is cleared when data is being been written to the transmitter FIFO.	1

			'0' – Otherwise	
7	Reserved	RO	Reserved	

Modem Status Register MSR (0x8808)

The register displays the current state of the modem control lines.

Bit	Name	Access	Description	Default
3-0	Reserved	RO	Reserved	
4	CTS input	RO	CTS input or equals to RTS in loopback mode.	0
5	DSR input	RO	DSR input or equals to DTR in loopback mode.	0
6	RI input	RO	RI input or equals to Out1 in loopback mode.	0
7	DCD input	RO	DCD input or equals to Out2 in loopback mode.	0

UART_TX FIFO Status (0x8809)

Bit	Name	Access	Description	Default
7-0	TX_FIFO_CNT	RO	TX FIFO available space counter	FFh

UART_RX FIFO Status (0x880a)

Bit	Name	Access	Description	Default
7-0	RX_FIFO_CNT	RO	RX FIFO occupied space counter	00h

UART_Clock Divisor Registers

In addition, there are 2 Clock Divisor registers that together form one 16-bit.
The registers can be accessed when the 7th (DLAB) bit of the Line Control Register is set to '1'. At this time the above registers UART_Receiver Buffer, UART_Transmit Buffer & UART_Interrupt Enable can't be accessed.

(Input Clock Speed)/(Divisor Latch value) = 16 x the communication baud rate

UART_Clock Divisor Registers_L (0x880b)

Bit	Name	Access	Description	Default
7-0	UART_Clock Divisor Registers_L	RW	UART_Clock Divisor Registers_low byte.	00h

UART_Clock Divisor Registers_H (0x880c)

Bit	Name	Access	Description	Default
7-0	UART_Clock Divisor Registers_H	RW	UART_Clock Divisor Registers_high byte.	00h

6 Electrical Characteristics

6.1 Absolute Maximum Rating

Symbol	Conditions	Minimum	Typical	Maximum
Supply Voltage		3.0 V	3.3V	3.6V
Storage Temp		-55°C		125°C

6.2 Power Dissipation

Operating Condition	Power consumption (W)
Unlink	0.386W
100M / active	0.558W
10M / active	0.398W

6.3 DC Characteristic

6.3.1 Operating Condition

Symbol	Conditions	Minimum	Typical	Maximum
PVDD	3.3V Supply voltage 2.5V Supply voltage	3.0 V 2.25V	3.3V 2.5V	3.6V 2.75V
CVDD	2.5V Supply voltage	2.25V	2.5V	2.75V
AVDD	2.5V Supply voltage	2.25V	2.5V	2.75V
ADC_VCC	2.5V Supply voltage	2.25V	2.5V	2.75V
VPP	2.5V Supply voltage (normal mode) 6.5V Supply voltage (write mode)	2.25V 6.25V	2.5V 6.5V	2.75V 6.75V
TA	Operating Temperature	0°C		70°C

6.3.2 ADC Operating Condition

Symbol	Conditions	Minimum	Typical	Maximum
ADC0	See Note.	0V		ADC_VCC
ADC1		0V		ADC_VCC
ADC_REFH		1.8V	2.0V	2.2V
ADC_REFL		0.4V	0.5V	0.6V

Note. The ADC input range,0~ADC_VCC, correspond to upper reference voltage, ADC_REFH, which is 4/5*ADC_VCC, and lower reference voltage, ADC_REFL,which is 1/5*ADC_VCC, would convert full range output code. When input is ADC_VCC, ADC convert 01111111, and input is 0V ADC convert 10000000. The output code represents in 2's-complement.

6.3.3 Supply Voltage

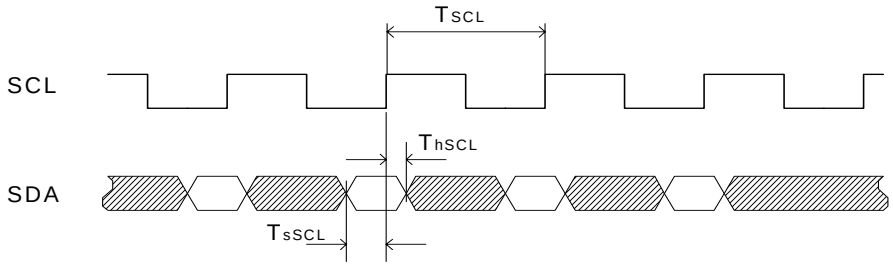
Symbol	Specific Name	Condition	Min	Max
V_{IH}	Input High Vol.		0.57*PVDD	
V_{IL}	Input Low Vol.			0.35*PVDD
V_{OH}	Output High Vol.		0.9*PVDD	
V_{OL}	Output Low Vol.			0.1*PVDD

6.4 AC Timing

6.4.1 EEPROM Timing

a.

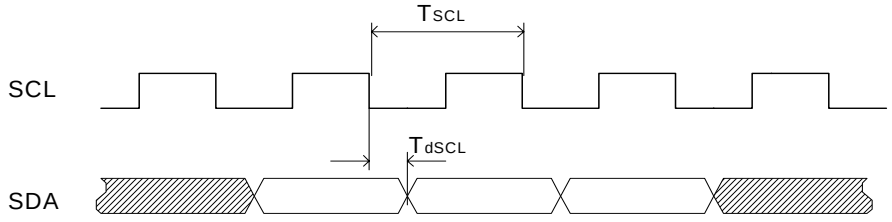
Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Receive clock period	-	20480	-	ns
T_{sSCL}	SDA to SCL setup time	2	-	-	ns
T_{hSCL}	SDA to SCL hold time	0.5	-	-	ns



Read data cycle

b.

Symbol	Description	Min.	Typ.	Max.	Unit
T_{SCL}	Transmit clock period	-	20480	-	ns
T_{dSCL}	SCL falling edge to SDA	-	-	5200	ns



Comand cycle

6.5 Thermal Data

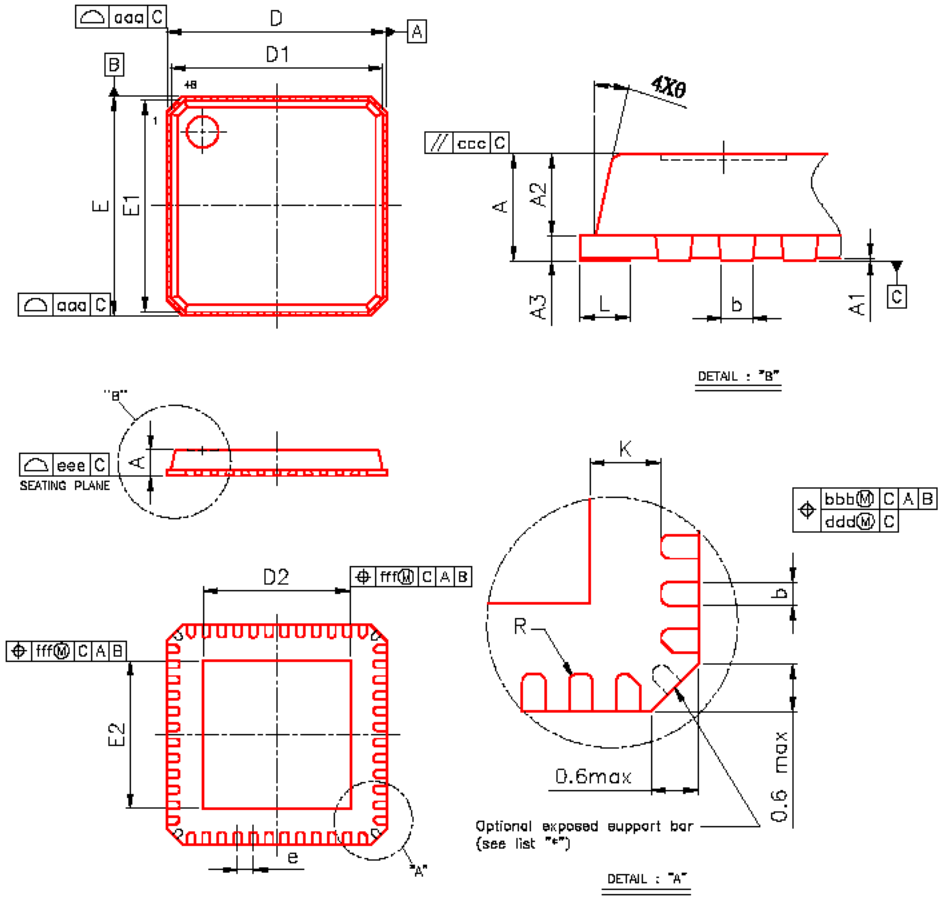
Theta Ja	Theta Jc	Conditions	Units
67.9	15.1	2 Layer PCB	^{o}C/W

7 Order Information

Part No.	Package	Notice
IP210T LF	48-PIN QFN	Lead free

8 Package Detail

Package and Mechanical Specification
IP210T-48 PIN (**48L QFN(7X7)**)



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	0.60	0.65	0.70	0.024	0.026	0.028
A3	0.20 REF			0.008 REF		
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	7.00 BSC			0.276 BSC		
D1/E1	6.75 BSC			0.266 BSC		
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	14°	0°	---	14°
R	0.09	---	---	0.004	---	---
K	0.20	---	---	0.008	---	---
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002
eee	---	---	0.08	---	---	0.003
fff	---	---	0.10	---	---	0.004

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT : JEDEC MO-220.

Exposed Pad Size							
L/F	D2/E2 (mm)			D2/E2 (inch)			*
	MIN	NOM	MAX	MIN	NOM	MAX	
①	4.90	5.05	5.20	0.193	0.199	0.205	NO
②	4.95	5.10	5.25	0.195	0.201	0.207	YES / NO
③	5.31	5.46	5.61	0.209	0.215	0.221	NO
④	3.56	3.71	3.86	0.140	0.146	0.152	NO
⑤	2.95	3.10	3.25	0.116	0.122	0.128	NO

IC Plus Corp.

Headquarters
10F, No.47, Lane 2, Kwang-Fu Road, Sec. 2,
Hsin-Chu City, Taiwan 300, R.O.C.
TEL : 886-3-575-0275 FAX : 886-3-575-0475
Website : www.icplus.com.tw

Sales Office
4F, No. 106, Hsin-Tai-Wu Road, Sec.1,
Hsi-Chih, Taipei Hsien, Taiwan 221, R.O.C.
TEL : 886-2-2696-1669 FAX : 886-2-2696-2220